M5L 2101A P, S; P-2, S-2; P-4, S-4

1024-BIT (256-WORD BY 4-BIT) STATIC RAM

DESCRIPTION

This is a family of 256-word by 4-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. These devices operate by a single 5V supply, as does TTL, and are directly TTL-compatible.

FEATURES

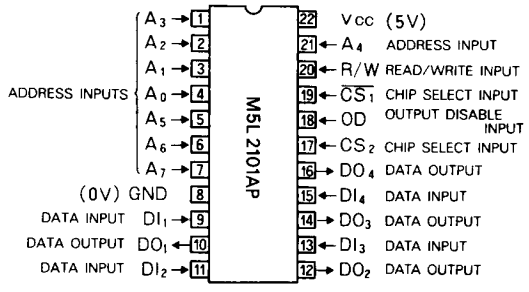
Parameter	M5L2101AP,S-2	M5L 2101AP,S	M5L2101AP,S-4
Access time (max)	250ns	350ns	450ns
Cycle time (min)	250ns	350ns	450ns

- Low power dissipation: 150μW/bit (typ)
- Single 5V supply voltage
- Data holding at 1.5V supply voltage (optional)
- No clocks or refreshing required
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state, with OR-tie capability
- Simple memory expansion by chip select input
- Separate data inputs and outputs
- Interchangeable with Intel's 2101A series in pin configuration and electrical characteristics

APPLICATION

- Small-capacity memory units

PIN CONFIGURATION (TOP VIEW)



Outline 22P1 (M5L2101AP)
22S1 (M5L2101AS)

FUNCTION

These devices provide separate data input and output terminals. During a write cycle, when a location is designated by address signals A_0~A_7 and signal R/W goes low, the data of the IN signal at that time is written.

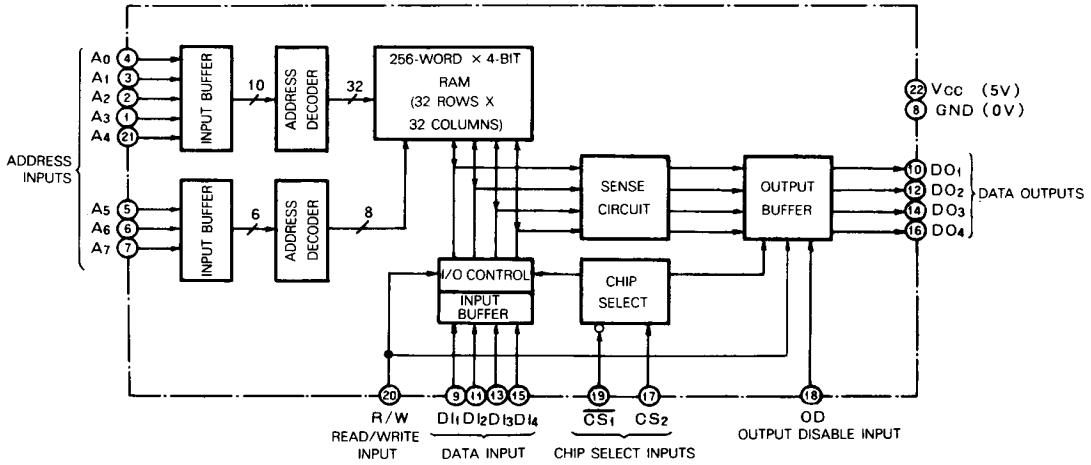
During a read cycle, when a location is designated by address signals A_0~A_7 and R/W goes high, data of the designated address is available at the DO terminal.

When signal $\overline{CS_1}$ is high or CS_2 is low, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state useful for OR-ties with other output terminals.

When signal OD is high, the output is in the floating state, so that OD is used as an input/output select control signal for common input/output operation.

The memory data can be held at a supply voltage of 1.5V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

BLOCK DIAGRAM



1024-BIT (256-WORD BY 4-BIT) STATIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage		With respect to GND	−0.3～7	V
V_I	Input voltage			−0.3～7	V
V_O	Output voltage			−0.3～7	V
Pd	Maximum power dissipation	M5L 2101AP	Ta＝25°C	700	mW
		M5L 2101AS		1000	mW
Topr	Operating free-air ambient temperature range			0～70	°C
Tstg	Storage temperature range	M5L 2101AP		−40～125	°C
		M5L 2101AS		−65～150	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝0～10°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IL}	Low-level input voltage	0		0.8	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{OH}	High-level output voltage	I_{OH}＝−200μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}＝3.5mA			0.45	V
I_I	Input current	V_I＝0～5.25V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS_1})}$＝2.2V, V_O＝2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS_1})}$＝2.2V, V_O＝0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I＝5.25V (all inputs), output open, Ta＝25°C		30	60	mA
C_i	Input capacitance, all inputs	V_I＝GND, f＝1MHz, 25mVrms		3	5	pF
C_o	Output capacitance	V_O＝GND, f＝1MHz, 25mVrms		8	12	pF

Note 1 : Current flowing into an IC is positive; out is negative.

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5L 2101AP, S-2			M5L 2101AP, S			M5L 2101AP, S-4			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	250			350			450			ns
$t_{a(AD)}$	Address access time			250			350			450	ns
$t_{a(CS)}$	Chip select access time			180			180			180	ns
$t_{a(OD)}$	Output disable access time			130			150			150	ns
t_{PXZ}	Output disable time (Note 3)			100			100			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	40			40			40			ns

Note 2 : Test conditions : input pulse V_{IH}＝2.2V, V_{IL}＝0.8V t_r＝t_f＝20ns ; reference level ＝1.5V; load＝2TTL, C_L＝100pF

Note 3 : t_{PXZ} is with respect to $\overline{CS_1}$, CS_2, or OD, whichever occurs first.

TIMING REQUIREMENTS (For Write Cycle) (Ta＝0～70°C, V_{CC}＝5V±5%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5L 2101AP, S-2			M5L 2101AP, S			M5L 2101AP, S-4			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	170			220			270			ns
$t_{w(WR)}$	Write pulse width	150			200			250			ns
$t_{su(AD)}$	Address setup time with respect to write	20			20			20			ns
t_{wr}	Write recovery time	0			0			0			ns
$t_{su(OD)}$	Output disable setup time with respect to data in	20			20			20			ns
$t_{su(DA)}$	Data setup time	100			150			170			ns
$t_{h(DA)}$	Data hold time	0			0			0			ns
$t_{su(CS)}$	Chip select setup time	150			200			250			ns

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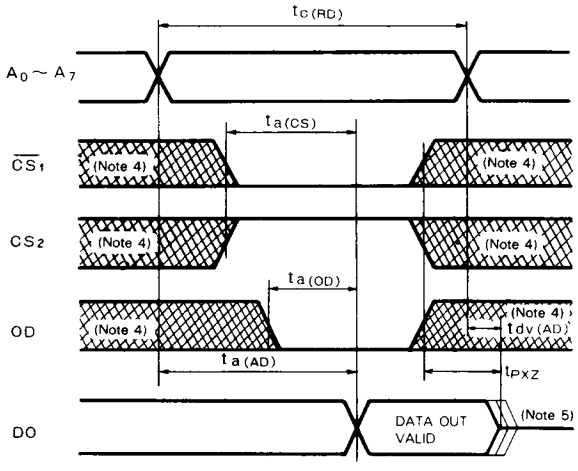
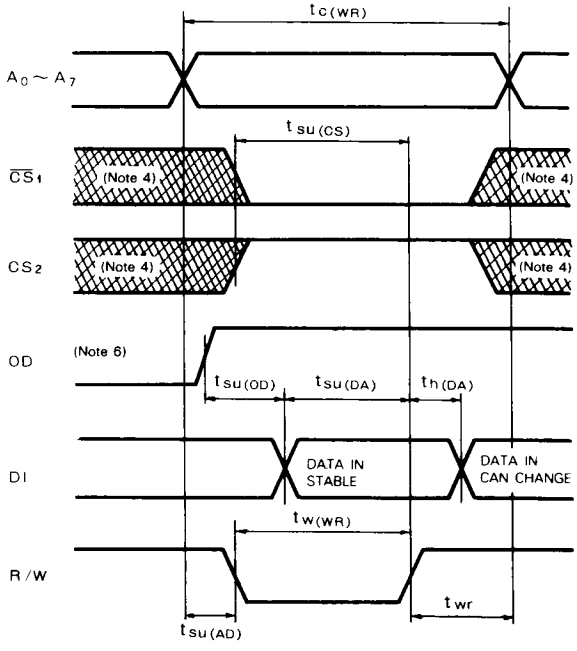
TIMING DIAGRAMS

Read Cycle



Write Cycle



Note 4 : Hatching indicates the state is unknown.

5 : Indicates that during this period the data out is invalid for this definition of $t_{dv(AD)}$ and is in the floating state for this definition of t_{PXZ}.

6 : OD may be kept low for the full cycle except during common input/output operation.

POWER-DOWN OPERATION (OPTIONAL) These characteristics are guaranteed only under custom specifications.

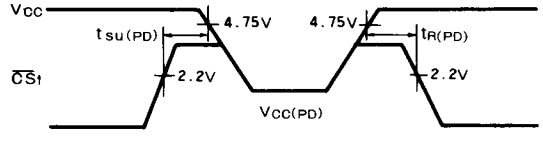
Electrical Characteristics (T_a = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		1.5			V
$V_I(\overline{CS1})$	Power-down chip select input voltage	2.2V ≦ $V_{CC(PD)}$ ≦ V_{CC}	2.2			V
		1.5V ≦ $V_{CC(PD)}$ ≦ 2.2V	$V_{CC(PD)}$			V
$I_{CC(PD1)}$	Power-down supply current from V_{CC}	V_{CC} = 1.5V, all inputs = 1.5V		15	30	mA
$I_{CC(PD2)}$	Power-down supply current from V_{CC}	V_{CC} = 2.0V, all inputs = 2.0V		20	40	mA

Timing Requirements (T_a = 0 ~ 70°C, V_{CC} = 5V ± 5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time		0			ns
$t_{R(PD)}$	Power-down recovery time		$t_{c(RD)}$			ns

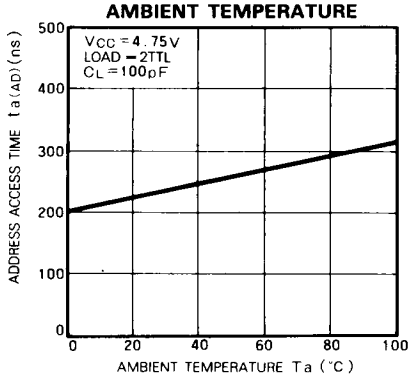
Timing Diagram



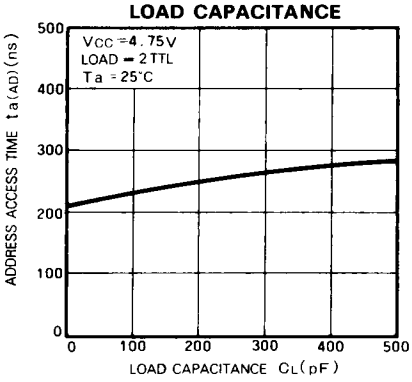
1024-BIT (256-WORD BY 4-BIT) STATIC RAM

TYPICAL CHARACTERISTICS

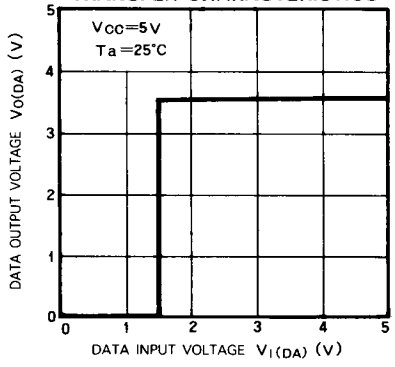
ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



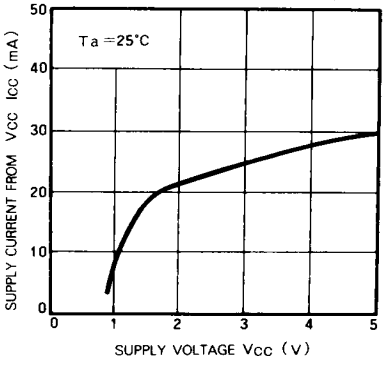
ADDRESS ACCESS TIME VS. LOAD CAPACITANCE



DATA INPUT/OUTPUT TRANSFER CHARACTERISTICS



SUPPLY CURRENT FROM Vcc VS. SUPPLY VOLTAGE Vcc



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